PATENT APPLICATION
DOCKET NO.: 200209001-1

REMARKS

Claims 1-23 are presented for examination, of which claims 1, 10, and 19 are in independent form.

Claims 1, 9, 10, 18-20, 22, and 23 are amended by way of the present response. Support for the amendments may be found in the original patent application in respect of FIGS. 3, 5 and 6, as well as associated description in the specification at Paragraphs [0023] and [0037]-[0041], *inter alia*.

Favorable reconsideration of the present application as currently constituted is respectfully requested in light of the amendments and arguments herein.

Regarding Amendments to the Specification

In the present Office Action, the disclosure is objected to because of certain informalities in several paragraphs. Accordingly, paragraphs [0002], [0021], and [0022] of the original specification have been appropriately amended to include the missing application numbers and filing dates of the related patent applications identified therein.

Regarding Claim Objections - Informalities

Claims 19 and 20 are objected to in the pending Office Action because of certain informalities. Applicant respectfully submits that these objections have been overcome or otherwise rendered moot by way of the present response wherein claims 19 and 20 have been amended appropriately.

Regarding the Claim Rejections - 35 U.S.C. §112

Claims 9, 18, and 23 are rejected in the pending Office Action under 35 U.S.C. §112, second paragraph, as being indefinite for lack of proper antecedent basis. In response, claims 9, 18, and 23 have been amended appropriately. It is therefore believed that the pending §112 rejections have been overcome or otherwise rendered moot.

Regarding the Claim Rejections - 35 U.S.C. §102(b)

Claims 1, 2, 4-7, 10, 11, 13-16, 19, 20, and 21 are rejected in the pending Office Action under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,887,003 to Ranson et al. (hereinafter the *Ranson* reference). In connection with these

rejections, the Examiner has commented as follows with respect to base claims 1, 10, and 19:

> Claims 1, 10, and 10:
>
> Ranson teaches the method of claim 19 and the zeroing circuit (Fig. 12, programmable state machine entry) to execute this method for a general purpose performance counter ("GPPC") (Fig. 13, counters 0-3) connected to a bus carrying debug data (Figs. 11 and 12, state machine input bus 1110). Ranson also teaches the zeroing circuit comprises logic for zeroing out a specified number of most significant bits ("MSBs") (Fig. 12, OR 1218, AND 1220, exclusive OR 1221, AND 1222) of a selected portion of the debug data (Fig. 12, via element 1202 (bit-wise select)) based on a mask generated by a mask generator block (Fig. 12, storage element 1204 (bit- wise mask)) and means for providing a selection control signal (storage elements 1201-1210 would be loaded with data by writing to state machine/counters control register circuitry 346) to the mask generator block (storage element 1204), the selection control signal operating to select the specified number of MSBs for zeroing. (Col. 15, l. 19 to col. 16, l. 49).

Applicant respectfully submits that these rejections have been overcome or otherwise rendered moot by way of the present response and offers the following discussion as support. As set forth in base claim 1, an embodiment of the present patent application is directed to a zeroing circuit for use in a general purpose performance counter connected to a bus carrying debug

data. The zeroing circuit comprises, *inter alia*, logic for zeroing out a specified number of most significant bits ("MSBs") of a selected portion of the debug data based on a mask generated by a mask generator block, wherein the logic for zeroing is operable to produce a multi-bit result. Also included is means for providing a selection control signal to the mask generator block, the selection control signal operating to select the specified number of MSBs for zeroing.

Similarly, base claim 10 is directed to another embodiment of a zeroing circuit operable in a general purpose performance counter connected to a bus carrying debug data. The claimed embodiment comprises, *inter alia*, means for providing a signal specifying a number of most significant bits ("MSBs") of a selected portion of the debug data to be zeroed out and means for zeroing out the specified number of MSBs of the selected portion of the debug data based on the signal to form a result.

Base claim 19 is directed to an embodiment of a method of implementing a zeroing circuit for general purpose performance counter connected to a bus carrying debug data. The claimed method involves, *inter alia*, generating a control signal

indicative of a number of most significant bits ("MSBs") of a selected portion of the debug data to be set to zero, creating an S-bit mask based on the control signal, and generating an S-bit zeroed data signal using the S-bit mask, wherein the S-bit zeroed data signal comprises the selected portion of the debug data with the indicated number of MSBs set to zero.

The *Ranson* reference is directed to a scheme for comparing a group of multi-bit binary fields with a multi-bit expected pattern to generate a set of final match results. For each multi-bit binary field, *Ranson* compares the field with the expected pattern, generates mask results that select the desired portion of the result, and creates preliminary match results equal to a logical ANDing of all bits making up the bitwise mask result. Secondary match results may be generated by negating all of the preliminary match results and final

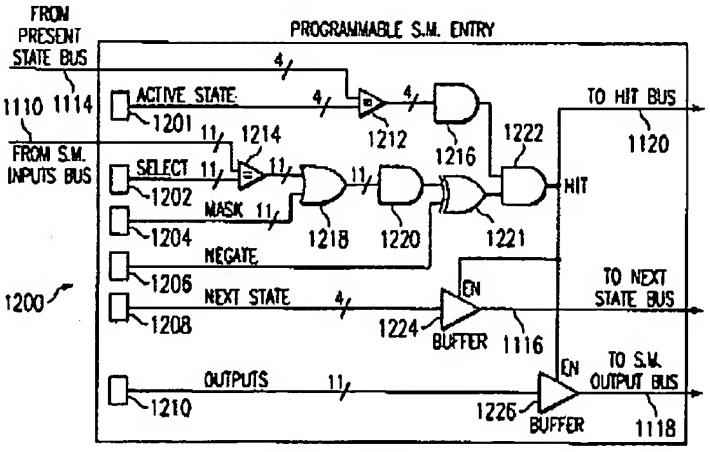

FIG. 12

match results are generated by individually gating all of the secondary match results with separate enable indicators. See Abstract. To achieve these actions, the *Ranson* reference contains a number of programmable state machine entries, such as the cited programmable state machine entry shown in FIG. 12, reproduced herein for convenience.

With regard to FIG. 12, *Ranson* discloses that the contents of storage element 1202 (bit-wise select) are compared with the eleven bits of state machine input bus 1110 by comparator 1214. The output bits of comparator 1214 is ORed at OR gate 1218 with the mask contained in storage element 1204 (bit-wise mask). The bit-wise results of this masking operation are ANDed together at AND gate 1220, resulting in a single-bit match result for the state machine input bus. At XOR gate 1221, the output of AND gate 1220 and a negate bit stored block 1206 are combined to provide a selectable inversion function. See column 15, lines 19-55.

Although a mask is used in this process, at no point during the process is there a result in which a specified number of most significant bits have been zeroed, thereby generating a multi-bit

zeroed data signal, as is recited in base claims 1, 9, and 19. The *Ranson* reference discloses using an OR gate to mask the results of comparator 1214, which means that the mask would force bits to one, not to zero. After OR gate 1218, AND gate 1220 gives a single-bit result, with a single-bit result also produced by XOR gate 1221 and AND gate 1222.

Based on the foregoing, Applicant respectfully submits that base claims 1, 10, and 19 are not anticipated or suggested by the applied art of record, and are therefore in condition for allowance. Claims 2 and 4-7 depend from base claim 1, claims 11 and 13-16 depend from base claim 10, and claims 20 and 21 depend from base claim 19, wherein each of these dependent claims introduces additional limitations in their respective base claims. Accordingly, these dependent claims are also believed to be allowable.

Regarding the Claim Rejections - 35 U.S.C. §103(a)

Claims 3, 8, 9, 12, 17, 18, 22 and 23 are rejected in the pending Office Action under 35 U.S.C. §103(a) as being unpatentable over the *Ranson* reference.

Each of the claims identified in the foregoing rejections under §103(a) depends from one of base claims 1, 10, and 19 and includes the same distinctions as do their respective base claims. As set forth above, the *Ranson* reference is insufficient when applied as a primary reference against the base claims. Reliance on mere official notice, however, is of no avail since it does not address the critical deficiencies of *Ranson*. Accordingly, dependent claims 3, 8, 9, 12, 17, 18, 22 and 23 are also believed to be allowable over *Ranson*.

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SUMMARY AND CONCLUSION

In view of the fact that none of the art of the record, whether considered alone or in combination discloses, anticipates or suggests the pending claims and in further view of the above remarks and/or amendments, reconsideration of the Action and allowance of the present patent application are respectfully requested and are believed to be appropriate.

Respectfully submitted,

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